Claims

1. A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, a lower surface, and at least one contact pad at said upper surface;

a structural material surrounding the at least one side surface of each chip of said plurality of chips and mechanically interconnecting in spaced, planar relation said plurality of chips, said structural material having an upper surface substantially co-planar with an upper surface of each chip of said plurality of chips to form a first substantially co-planar surface, said first substantially co-planar surface comprising a front surface, and such that a lower surface of said structural material is substantially parallel with a lower surface of each chip of said plurality of chips to form a second surface, said second surface comprising a back surface; and

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material mechanically interconnecting said plurality of chips, said in situ processed layer including via openings to at least some contact pads at the upper surfaces of said plurality of chips for electrical connection thereto.

2. The multichip module of claim 1, wherein said structural material has a thickness equal to a thickest chip of said plurality of chips such that the upper surface of the structural material is substantially co-planar with the upper surface of the thickest chip to form said first substantially co-planar surface, and such that a lower surface of the structural material is substantially co-planar with a lower surface of said thickest chip of said plurality of chips to form a second substantially co-planar surface, said second substantially co-planar surface comprising said back surface.

~~2~~ 3. The multichip module of claim 1, further comprising an intrachip metallization layer comprising metallization within each via opening electrically connected to a corresponding contact pad of said at least some contact pads, wherein metallization over each chip is isolated from metallization over each other chip of said plurality of chips such that said intrachip metallization layer fails to electrically interconnect any chips of said plurality of chips.

37

Subj 4. The multichip module of claim 1, wherein each chip of said plurality of chips has a common thickness, and wherein said structural material surrounding and mechanically interconnecting said chips in spaced planar relation comprises a thickness equal to said common thickness of said plurality of chips such that said second surface comprises a second substantially co-planar surface wherein the lower surface of said structural material is substantially co-planar with the lower surface of each chip of said plurality of chips, and wherein said first substantially co-planar surface comprising said front surface is parallel to said second substantially co-planar surface comprising said back surface.

3 5. The multichip module of claim 1, further comprising a multi-layer structure disposed over said in situ processed layer, said multi-layer structure including a chip interconnect metallization layer electrically interconnecting at least some chips of said plurality of chips.

Subj 3 6. The multichip module of claim 5, wherein said multi-layer structure further comprises a release layer disposed over said in situ processed layer, said release layer being thermally or chemically removable without removing said in situ processed layer.

38

5 11. The multichip module of claim 4, wherein said release layer comprises a thermoplastic transition layer disposed on said in situ processed layer, said release layer being removable with application of heat to said thermoplastic transition layer.

6 8. The multichip module of claim 3, wherein said multi-layer structure comprises a first multi-layer structure and is disposed over said in situ processed layer on said front surface, and said multichip module further comprises a second multi-layer structure disposed over said back surface.

7 9. The multichip module of claim 6, wherein said second multi-layer structure comprises a preprocessed printed circuit board conductively secured to said back surface.

8 10. The multichip module of claim 6, further comprising at least one conductive through connect disposed within said structural material and extending between said front surface and said back surface for facilitating electrical interconnection of said first multi-layer structure and said second multi-layer structure.

9 11. The multichip module of claim 8, further comprising at least one surface mount electronic component disposed on an exposed surface of at least one of said first multi-layer structure and said second multi-layer structure.

10 9
12. The multichip module of claim 11, wherein said at least one surface mount electronic component comprises a first surface mount electronic component disposed on an exposed surface of said first multi-layer structure and a second surface mount electronic component disposed on an exposed surface of said second multi-layer structure, said first surface mount electronic component and said second surface mount electronic component being electrically coupled through said at least one conductive through connect in said structural material.

11
13. The multichip module of claim 1, wherein at least one chip of said plurality of chips comprises a bare integrated circuit chip.

12
14. The multichip module of claim 1, wherein each chip of said plurality of chips comprises a bare integrated circuit chip.

Subj
15. The multichip module of claim 14, wherein each chip of said plurality of chips has an equal thickness such that the upper surface of each chip is co-planar with said front surface and the lower surface of each chip is co-planar with said back surface, said back surface comprising a planar main surface of the multichip module.

19 18
16. The multichip module of claim 15, further comprising a heat sink in physical contact with said back surface.

13

17. The multichip module of claim 1, wherein said in situ processed layer disposed on said front surface comprises a photo-patternable dielectric material.

14 13

18. The multichip module of claim 17, wherein said structural material comprises a polymer consisting of one of epoxy, urethane and polyimide.

19. An integrated circuit chip module comprising:

an integrated circuit chip comprising a bare chip having a substrate, active circuitry associated with said substrate, an upper surface and a lower surface, said integrated circuit chip further comprising multiple electrical contact pads at said upper surface electrically coupled to said active circuitry, said integrated circuit chip further having at least one side with a width defined by said upper surface and said lower surface;

a structural material surrounding said at least one side of said integrated circuit chip, said structural material having a top surface substantially co-planar with said upper surface of said integrated circuit chip to form a first surface, said first surface comprising a front surface, and said structural material having a bottom surface substantially parallel with said lower surface of said integrated circuit chip to form a second surface, said second surface comprising a back surface;

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material surrounding said at least one side of said integrated circuit chip, said in situ processed layer including at least one via opening to at least one contact pad of said multiple electrical contact pads at the upper surface of said integrated circuit chip; and

a metallization structure comprising metallization disposed within said at least one via opening electrically connecting to said at least one contact pad of said integrated circuit chip.

21 ~~20~~. The integrated circuit chip module of claim 20 ~~19~~, wherein said in situ processed layer comprises a photo-patternable dielectric material.

22 ~~21~~. The integrated circuit chip module of claim 21 ~~20~~, wherein said structural material comprises a polymer consisting of one of epoxy, urethane and polyimide.

23 ~~22~~. The integrated circuit chip module of claim 21 ~~20~~, wherein said metallization structure further comprises at least one input/output (I/O) contact at an exposed surface of said module, said at least one I/O contact being electrically coupled to said at least one contact pad of said integrated circuit chip, and being disposed at least partially over said structural material surrounding said at least one side of said integrated circuit chip.

Subj ~~23~~. The integrated circuit chip module of claim 20, wherein said bottom surface is substantially co-planar with said lower surface of said integrated circuit chip.

24. The integrated circuit chip module of claim 20, wherein said back surface comprises an exposed planar main surface of said integrated circuit chip module.

42

25. A method for fabricating a multichip module comprising the steps of:

(a) providing a plurality of chips, each chip comprising a bare chip having at least one side, an upper surface, a lower surface, and a contact pad at said upper surface;

(b) placing said plurality of chips on an alignment carrier in spaced relation with the upper surfaces thereof facing said alignment carrier;

(c) surrounding said plurality of chips with a structural material such that said at least one side of each chip is covered by said structural material, an exposed surface of said structural material being substantially parallel with the lower surfaces of said said plurality of chips, thereby defining a back surface; and

(d) affixing said back surface to a process carrier, and separating said alignment carrier from said plurality of chips.

26. The method of claim 25, further comprising forming metallization structures above said plurality of chips to electrically interconnect said chips.

27. The method of claim 25, further comprising forming by in situ processing a dielectric layer on the upper surfaces of said plurality of chips and an upper surface of said structural material substantially co-planar therewith.

28. The method of claim 27, further comprising patterning and forming vias in said in situ formed dielectric layer, said vias being disposed to expose at least some contact pads at the upper surfaces of the plurality of chips for facilitating electrical connection thereto.

29. The method of claim 26, further comprising forming metallization structures above said in situ formed dielectric layer, said metallization structures comprising metallization within said vias electrically connected to at least some contact pads exposed by said vias.

30. The method of claim 29, wherein said forming of said metallization structures comprises forming intrachip metallization within said vias electrically connected to at least some contact pads exposed by said vias, wherein intrachip metallization over each chip is isolated from intrachip metallization over each other chip of said plurality of chips such that said intrachip metallization structures individually fail to electrically interconnect any two chips of said plurality of chips.

31. The method of claim 27, wherein said surrounding step (c) includes surrounding said plurality of chips with the structural material such that the at least one side surface and the lower surface of each chip is covered by the structural material, and removing structural material from the exposed surface of the structural material until said structural material has a thickness equal to at least one chip of said plurality of chips, the exposed surface of said structural material being co-planar with the lower surface of said at least one chip.

32. The method of claim 31, wherein said removing comprises lapping said exposed surface until said structural material has a thickness equal to said thickness of said at least one chip of said plurality of chips.

33. The method of claim 32, wherein said lapping comprises lapping said exposed surface until the lower surfaces of said plurality of chips and said exposed surface of said structural material are co-planar.

34. The method of claim 27, wherein said forming step (e) comprises forming a photo-patternable dielectric layer on the upper surfaces of the plurality of chips and the upper surface of the structural material, said photo-patternable dielectric layer comprising said in situ formed dielectric layer.

35. The method of claim 34, wherein the structural material of said surrounding step (c) comprises a polymer consisting of one of epoxy, urethane, and polyimide.

36. The method of claim 33, wherein said surrounding step (c) comprises:

(i) applying said polymer until said at least one side of each chip is covered by said polymer and said polymer has a thickness at least equal to a thickness of a thickest chip of said plurality of chips;

(ii) curing said polymer; and

(iii) lapping said polymer from an exposed surface at least until said exposed surface of said polymer and a lower surface of said thickest chip of said plurality of chips are co-planar, thereby defining said back surface.

37. The method of claim 27, wherein said placing step (b) includes securing said plurality of chips to said alignment carrier via an adhesive layer.

38. The method of claim 37, wherein said affixing step (d) includes providing a process carrier adhesive on said process carrier for affixing said back surface thereto, and applying a catalyst for said process carrier adhesive on said back surface such that said back surface is substantially instantaneously affixed to said process carrier upon physical contact with said process carrier adhesive.

39. The method of claim 27, further comprising providing a first multi-layer structure over said in situ formed dielectric layer, said first multi-layer structure including chip interconnect metallization electrically interconnecting at least some chips of said plurality of chips.

40. The method of claim 39, further comprising applying a release layer to said in situ formed dielectric layer prior to said providing of said first multi-layer structure, said release layer facilitating subsequent removal of said first multi-layer structure.

41. The method of claim 39, further comprising affixing at least one surface mount electronic component to an exposed surface of said first multi-layer structure such that said at least one surface mount electronic component is electrically connected to at least one chip of said plurality of chips.

42. The method of claim 39, further comprising providing a second multi-layer structure disposed over said back surface.

43. The method of claim 42, wherein said providing of said second multi-layer structure comprises providing said second multi-layer structure as a preprocessed printed circuit board and attaching said preprocessed printed circuit board to said back surface.

44. The method of claim 42, wherein said placing step (b) includes placing at least one conductive through connect die commensurate with placing of said plurality of chips such that said structural material of said step (c) surrounds a side of said at least one electrical through connect die, and wherein said at least one electrical through connect die electrically couples said first multi-layer structure and said second multi-layer structure.

45. The method of claim 44, further comprising a first surface mount electronic component affixed to an exposed surface of said first multi-layer structure and a second surface mount electronic component affixed to an exposed surface of said second multi-layer structure, said first surface mount electronic component and said second surface mount electronic component each being electrically coupled to at least one chip of said plurality of chips.

46. The method of claim 27, further comprising testing said plurality of chips for a defective chip and if identified, repairing said multichip module by replacing said defective chip.

47. The method of claim 46, wherein said repairing comprises:

(i) transferring said multichip module to an alignment plate by affixing said alignment plate to an exposed surface of said in situ formed dielectric layer and temporarily removing said process carrier from said plurality of chips;

(ii) removing a defective chip of said plurality of chips;

(iii) replacing the defective chip with a preprocessed chip of a same chip type as the defective chip; and

(iv) surrounding the preprocessed chip with structural material to physically bond the preprocessed chip to other chips of the plurality of chips in the multichip module.

48. The method of claim 47, wherein said removing of said defective chip comprises mechanically milling or laser ablating said structural material and said in situ formed dielectric layer about said defective chip to facilitate removal of said defective chip.

49. The method of claim 47, wherein said preprocessed chip has a thickness greater than said thickness of said structural material in said step (c) and said repairing further comprises subsequent to said replacing step (iii), lapping a back surface of said preprocessed chip to a thickness equal to said thickness of said structural material surrounding said plurality of chips in said step (c).

50. A method for forming a single chip module comprising employing said multichip module fabricating method of claim 29, and subsequent thereto, separating said plurality of chips in said multichip module such that a single chip module is formed for each chip of said plurality of chips.

51. A method for repairing the multichip module of claim 1, said method comprising the steps of:

(i) transferring said multichip module to an alignment plate by affixing said alignment plate to an exposed surface of said in situ processed layer;

(ii) removing a defective chip;

(iii) replacing the defective chip with a preprocessed chip of a same chip type as the defective chip; and

(iv) surrounding the preprocessed chip with structural material to physically bond the preprocessed chip to other chips of the plurality of chips in the multichip module.

52. The method of claim 51, wherein said removing of said step (ii) chip comprises mechanically milling or laser ablating said structural material and said in situ processed layer about said defective chip to facilitate removing of said defective chip.

53. The method of claim 51, wherein said preprocessed chip has a thickness greater than said thickness of said structural material surrounding said side surfaces of said plurality of chips, and wherein said method further comprises lapping a back surface of said preprocessed chip to a thickness equal to said thickness of said structural material surrounding said at least one side surface of each chip of said plurality of chips.

54. A method for repairing the multichip module of claim 5, said method comprising the steps of:

(i) removing said multi-layer structure disposed over said in situ processed layer;

(ii) affixing an exposed surface of said in situ processed layer to an alignment plate;

(iii) removing a defective chip;

(iv) replacing the defective chip with a preprocessed chip of a same chip type as the defective chip; and

(v) surrounding the preprocessed chip with structural material to physically bond the preprocessed chip to other chips of the plurality of chips in the multichip module.

55. The method of claim 54, wherein said removing said (iii) comprises mechanically milling or laser ablating said structural material and said in situ processed layer about said defective chip to facilitate said removing of said defective chip.

56. A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, and a lower surface; and

structural material surrounding the at least one side surface of each chip of said plurality of chips to mechanically interconnect in spaced planar relation said plurality of chips, said structural material having an upper surface co-planar with the upper surfaces of said plurality of chips, wherein a co-planar front surface is defined thereby, and wherein a lower surface of said structural material is substantially parallel with the lower surfaces of the plurality of chips, thereby defining a back surface.

57. The multichip module of claim 56, wherein each chip of said plurality of chips includes at least one contact pad at the upper surface thereof, said at least one contact pads being exposed at said co-planar front surface.

58. The multichip module of claim 56, wherein the lower surface of the structural material is substantially co-planar with the lower surfaces of the plurality of chips.

59. The multichip module of claim 58, wherein said back surface is adhesively secured to a heat sink.

* * * * *